4:1 BANDWIDTH DIGITAL FIVE BIT MMIC PHASE SHIFTERS

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ABSTRACT

Five bit MMIC phase shifters that cover over two octaves of bandwidth have been demonstrated. The phase shifters maintain low phase error, insertion loss, insertion loss variation with phase state, and VSWR, over their entire operational bandwidths.

INTRODUCTION

Phase shifters are required in many microwave systems for functions such as electronic beam steering and frequency translation. This paper describes digitally controlled MMIC phase shifters with performance levels immediately suitable for wideband applications. Two phase shifter designs are presented that use the same circuit approach but have been optimized for different operating bandwidths. A lowband version of the phase shifter was designed for the 2.0 to 6.0 GHz frequency range and a highband version was designed for the 4.5 to 18.0 GHz frequency range. Both versions maintain useful performance levels significantly beyond their design bandwidths.

The typical measured circuit performance of a highband phase shifter chip in the 4.5 to 18 GHz band shows a maximum phase error of less than 20° and a +/- 1.15 dB maximum change in insertion loss with phase state. The measured circuit performance of a lowband phase shifter chip in the 2.0 to 6.0 band shows a maximum phase error of less than 15° and less than +/- 0.6 dB insertion loss variation with phase state.

DESIGN

The 5 bit phase shifters were composed of four separately optimized phase shifter sections consisting of a 180 degree bit, a 90 degree bit, a 45 degree bit, and a combined 22.5/11.25 degree section. These sections were cascaded together directly in the five bit chip. The 11.25 and 22.5 degree functions were combined in one section to realize size and insertion loss savings over a separate bit approach. The block diagram and simplified schematic diagram of the five bit phase shifter is shown in figure 1. A photograph of the highband chip is shown in figure 2.

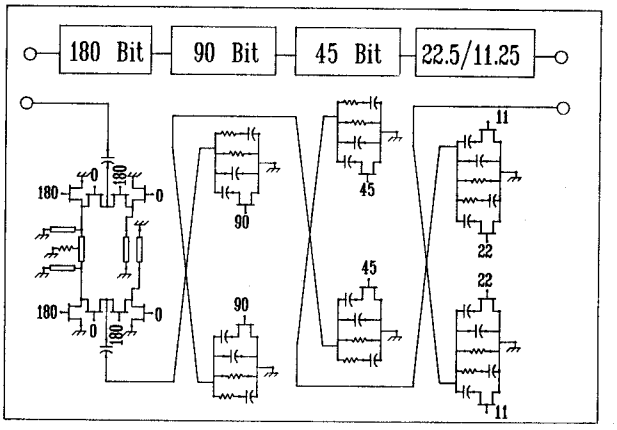

Figure 1. Block Diagram and Simplified Schematic Diagram of the Five Bit Phase Shifter

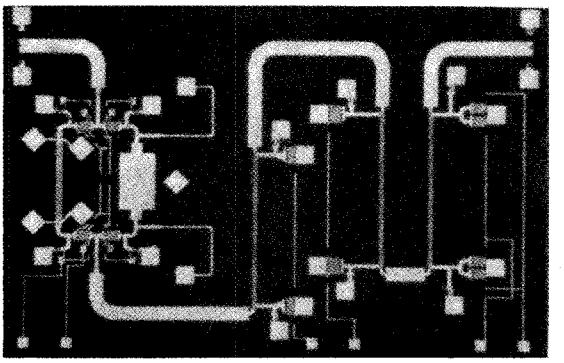

Figure 2. Photograph of Sanders Highband Phase Shifter Chip.

The topologies of the 90, 45, and 22.5/11.25 degree sections utilized interdigitated quadrature couplers terminated with FET switched reflective loads. The 22.5/11.25 degree section utilized termination networks with two FET switches each. In operation, the input signal to the coupler splits and is incident upon two identical terminations. Signals reflected from the terminations add at the output port of the coupler. Changes in the impedance of the reflective terminations cause both phase and amplitude variations at the output of the coupler.

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These impedance changes are introduced in this design by altering the state of the FET switches in the termination networks. The FET switches are operated in fully on-state and fully off-state conditions only. This allows direct digital control of the phase shifter and reduces chip-to-chip variations found in analog controlled designs using varactors.

The insertion loss of the phase shifter sections was minimized by making the terminations as reflective as possible. To reduce the incidental amplitude modulation of the phase shifter sections, a small amount of loss was deliberately introduced in the termination networks to equalize the magnitude of the reflection coefficients of the networks in each of their states.

The 180 degree bit designs were based on two circuit duals that possess an inherent 180 degree transmission phase difference for all frequencies, but otherwise behave identically as bandpass filters. The basic networks are a pi section of transmission lines and a coupled transmission line section described in reference 1. A FET SPDT switch arrangement was used to select the desired network. The amplitude modulation of the bit was minimized by the addition of a high value shunt resistor to the pi network section to compensate for the slightly higher loss of the coupled line section.

The use of a 10 mil thick substrate was necessary in order to achieve low loss performance from the interdigitated couplers over a two octave bandwidth. The 10 mil chip thickness permitted the fingers of the couplers to be made wide enough to be plated thereby minimizing the associated circuit losses. The use of a thicker substrate forced an extension of Sanders standard self-limiting plasma etched via hole process. This involved revising the design rules for the top side catch pads and via hole spacing. The availability of the via holes through the thicker substrate permitted the use of on-chip grounding in the circuit designs and also enabled the on-wafer RF probe evaluation of the chips. The increased chip thickness also enhanced the mechanical integrity of these chips whose edge dimensions are .320" x .210" for the highband design and .330" x .330" for the lowband design.

FABRICATION

The phase shifter chips were fabricated using Sanders 0.5 micron ion implanted self-aligned gate MMIC process. Sanders standard process includes ion implanted resistors, silicon nitride for MIM capacitors and device passivation, plated transmission lines, air bridges, and via holes through the substrate.

The switching elements used in the phase shifter were 0.5 micron FETs designed specifically for high isolation when biased off and minimal insertion loss when biased on. This was accomplished using Sanders' standard N+ over N ion implanted active layer with 0.5 micron gates. The gates were fabricated by contact lithography and were self-aligned to a narrow 1 micron recess through the N+ layer in a single photolithographic step. The isolation of these devices was increased by an interdigitated layout with minimized parasitic capacitance, resulting in 0.21 pF/mm of total off-state capacitance. The insertion loss was minimized by the 150 Ohm/square N+ layer in close proximity to the 0.5 micron gate, resulting in 2.4 Ohm-mm of on-state resistance. A total FET gate periphery of about 7.5 mm per chip was used in each of the two designs.

RESULTS

The measured circuit performance of a highband phase shifter chip in all 32 states is shown in figures 3-6. In the 4.5 to 18 GHz band, the chip measurements show an overall RMS phase error of 5.7 degrees, an overall RMS amplitude error of 0.36 dB, a maximum RMS phase error of 9.5 degrees, a maximum RMS amplitude error of 0.50 dB, an average insertion loss of 10.0 dB, and a maximum port VSWR of 2.13:1. The phase errors reported in this paper are defined with respect to one of the phase states of the phase shifter. The measured performance is summarized in Table I. The useful performance of the chip extends beyond the 4.5 to 18 GHz design bandwidth and exceeds a 5:1 bandwidth.

To quantify the effects of normal processing variations on the performance of the phase shifter design and to establish typical chip performance levels, the measured circuit performance of 46 highband phase shifter chips from 3 wafer lots was analyzed and is summarized in Table II. The unit to unit phase variations of the 46 phase shifters at the same phase state are plotted normalized to one of the devices in figure 7. The maximum standard deviation of these phase variations across the 4.5 to 18 GHz band is 9.5°.

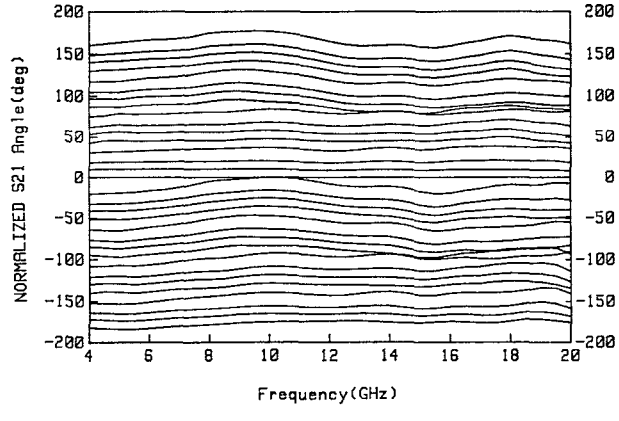

Figure 3. Measured Phase Shift of Highband Phase Shifter Chip in All 32 States.

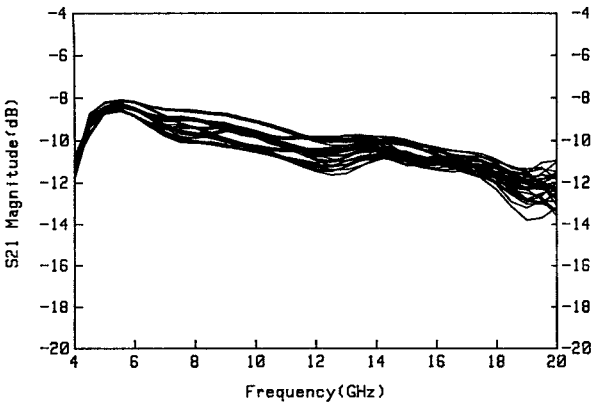

Figure 4. Measured Insertion Gain of Highband Phase Shifter Chip in All 32 States.

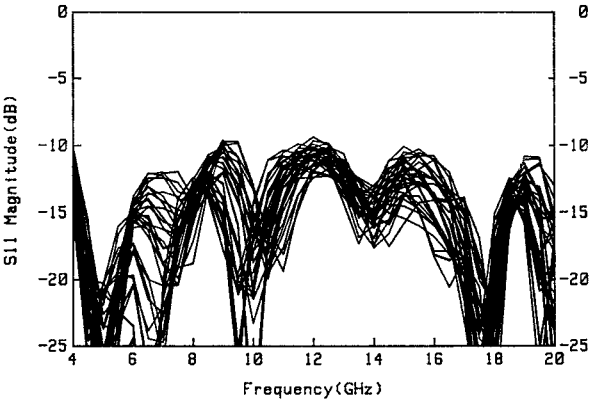

Figure 5. Measured S11 Magnitude of Highband Phase Shifter Chip in All 32 States.

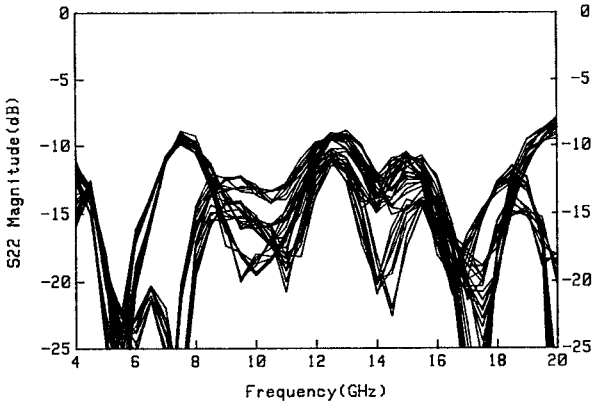

Figure 6. Measured S22 Magnitude of Highband Phase Shifter Chip in All 32 States.

TABLE I
Summary of Sanders Highband Phase Shifter Chip Performance.

DEVICE: 88-082-4 R=4 C=3 D=1
REFERENCED TO: 88-082-4 R=4 C=3 D=1 A=0
FREQUENCY RANGE 4500 TO 18000 MHz

FREQ MHz	AVE PHASE ERR°	RMS PHASE ERR°	MAX PHASE ERR°	MIN I.L. dB	AVE I.L. dB	MAX I.L. dB	MAX I.L. CHANGE	RMS I.L. ERR dB	MAX INPUT VSWR	MAX OUTPUT VSWR
4500	5.2	5.8	9.9	8.7	9.2	9.8	1.05	.31	1.40	1.62
5000	5.2	5.9	11.0	8.2	8.5	8.7	.56	.16	1.22	1.29
5500	4.6	5.3	9.2	8.1	8.3	8.6	.56	.17	1.38	1.17
6000	3.4	4.0	7.6	8.2	8.5	8.9	.72	.23	1.51	1.37
6500	2.6	3.1	6.1	8.4	8.9	9.4	.98	.29	1.67	1.52
7000	1.4	1.9	4.0	8.5	9.1	9.8	1.28	.34	1.68	1.82
7500	1.3	1.6	2.8	8.5	9.3	10.1	1.53	.41	1.68	2.12
8000	2.5	3.0	6.3	8.6	9.3	10.1	1.55	.44	1.64	2.05
8500	3.5	4.2	8.1	8.7	9.5	10.2	1.51	.41	1.83	1.75
9000	4.5	5.2	9.5	8.7	9.5	10.3	1.60	.43	2.00	1.63
9500	5.0	5.7	10.5	8.9	9.7	10.4	1.53	.45	1.98	1.65
10000	4.8	5.6	11.4	9.1	9.9	10.6	1.51	.44	1.59	1.59
10500	4.2	5.0	10.8	9.2	10.1	10.7	1.48	.42	1.78	1.55
11000	3.4	4.2	9.2	9.4	10.3	10.9	1.47	.42	1.88	1.60
11500	3.0	3.6	6.6	9.7	10.4	11.2	1.51	.45	1.95	1.79
12000	3.3	4.0	8.6	9.8	10.6	11.5	1.66	.48	2.04	1.97
12500	4.1	5.3	11.7	9.8	10.6	11.6	1.84	.50	1.96	2.10
13000	4.7	6.2	13.5	9.7	10.6	11.6	1.82	.48	1.84	2.13
13500	4.9	6.3	13.4	9.7	10.4	11.2	1.48	.41	1.63	1.93
14000	4.9	6.1	12.7	9.8	10.3	10.9	1.14	.32	1.58	1.67
14500	5.3	6.6	13.1	9.8	10.4	10.9	1.10	.31	1.77	1.79
15000	6.7	8.4	15.4	10.0	10.7	11.2	1.23	.36	1.92	1.85
15500	7.5	9.5	16.9	10.2	10.8	11.3	1.11	.35	1.89	1.82
16000	7.1	8.5	15.4	10.3	10.9	11.4	1.08	.28	1.82	1.65
16500	6.2	7.2	13.1	10.5	11.0	11.5	1.02	.24	1.68	1.39
17000	5.7	6.7	11.9	10.5	11.1	11.6	1.02	.26	1.51	1.35
17500	5.4	6.4	12.1	10.6	11.2	11.8	1.16	.30	1.33	1.45
18000	5.4	6.3	14.2	10.9	11.5	12.3	1.44	.34	1.43	1.60
	AVE 4.5	MAX 9.5	MAX 16.9	MIN 8.1	AVE 10.0	MAX 12.3	MAX 1.84	MAX .50	MAX 2.04	MAX 2.13

OVERALL RMS PHASE ERROR = 5.7°
OVERALL RMS AMPL ERROR = .36 dB

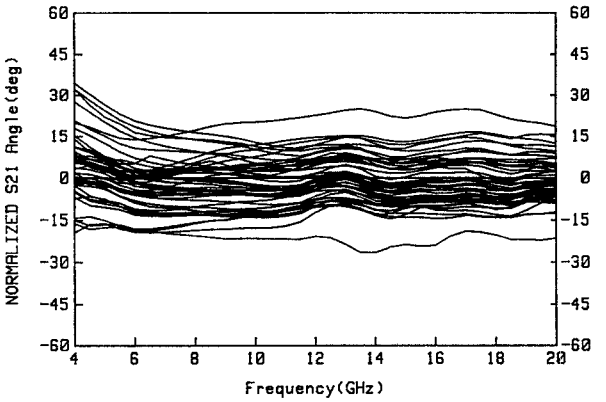

Figure 7. Measured Variation of Insertion Phase for Same State of 46 Chips (Normalized to One of the Chips).

TABLE II

Summary of Performance of 46 Highband Chips
4.5 - 18 GHz

PARAMETER	MEAN	STD DEV
Overall RMS Phase Error	6.4°	0.7°
Overall RMS Amplitude Error	0.44dB	0.08dB
Maximum Phase Error	19.9°	3.7°
Maximum RMS Phase Error	10.2°	1.3°
Minimum Insertion Loss	8.0dB	0.4dB
Average Insertion Loss	10.3dB	0.5dB
Maximum Insertion Loss	12.9dB	0.7dB
Max. Insertion Loss Change	2.3dB	0.4dB
Max. RMS Insertion Loss Error	0.61dB	0.11dB
Maximum Input VSWR	2.04	0.15
Maximum Output VSWR	2.24	0.14

The measured circuit performance of a lowband phase shifter chip in all 32 states is shown in figures 8-11. Over the 2.0 to 6.0 GHz band, the chip measurements show an overall RMS phase error of 4.4 degrees, an overall RMS amplitude error of 0.23 dB, a maximum RMS phase error of 7.6 degrees, a maximum RMS amplitude error of 0.33 dB, an average insertion loss of 7.6 dB, and a maximum port VSWR of 2.01:1. The useful performance of the chip extends to about a 4:1 bandwidth. The measured performance is summarized in Table III.

TABLE III
Summary of Sanders Lowband Phase Shifter
Chip Performance.

DEVICE: 88-062-1 R=2 C=3 T=1
REFERENCED TO: 88-062-1 R=2 C=3 T=1 A=0
FREQUENCY RANGE 2000 TO 6000 MHz

FREQ MHz	AVE PHASE ERR°	RMS PHASE ERR°	MAX PHASE ERR°	MIN I.L. dB	AVE I.L. dB	MAX I.L. dB	MAX I.L. CHANGE	RMS I.L. ERR dB	MAX INPUT VSWR	MAX OUTPUT VSWR
2000	6.5	7.6	14.1	6.7	7.2	7.8	1.09	.33	1.93	2.01
2250	3.9	4.8	9.0	6.2	6.6	7.1	.90	.30	1.39	1.68
2500	3.4	4.3	7.9	6.0	6.2	6.5	.50	.13	1.25	1.36
2750	2.7	3.5	6.0	6.0	6.3	6.5	.49	.13	1.40	1.34
3000	2.0	2.5	4.5	6.3	6.6	6.9	.56	.17	1.57	1.58
3250	1.6	2.0	4.0	6.7	7.0	7.3	.55	.21	1.70	1.63
3500	1.9	2.3	4.4	6.9	7.2	7.5	.63	.24	1.68	1.52
3750	2.6	3.2	7.0	7.0	7.3	7.7	.67	.24	1.56	1.57
4000	3.0	3.7	8.4	7.1	7.5	7.8	.70	.22	1.48	1.45
4250	3.2	3.9	8.9	7.3	7.6	8.0	.76	.23	1.53	1.54
4500	3.2	4.0	8.8	7.4	7.8	8.3	.85	.23	1.64	1.69
4750	3.3	4.2	8.8	7.6	8.1	8.5	.84	.24	1.68	1.80
5000	3.8	4.7	10.7	7.8	8.3	8.7	.86	.23	1.66	1.83
5250	4.2	5.2	11.9	8.1	8.5	8.9	.81	.23	1.58	1.77
5500	4.4	5.4	12.3	8.4	8.8	9.2	.81	.23	1.39	1.78
5750	4.5	5.5	12.3	8.6	9.1	9.5	.96	.25	1.47	1.93
6000	4.2	5.2	11.4	8.8	9.4	10.0	1.17	.28	1.57	1.94
	AVE	MAX	MAX	MIN	AVE	MAX	MAX	MAX	MAX	MAX
	3.4	7.6	14.1	6.0	7.6	10.0	1.17	.33	1.93	2.01

OVERALL RMS PHASE ERROR = 4.4°
OVERALL RMS AMPL ERROR = .23 dB

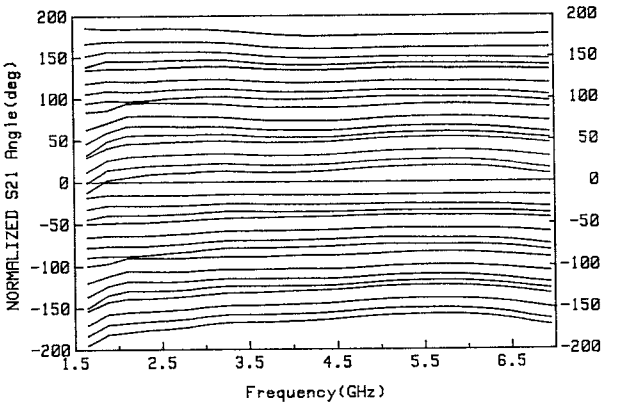

Figure 8. Measured Phase Shift of Lowband Phase Shifter Chip in All 32 States.

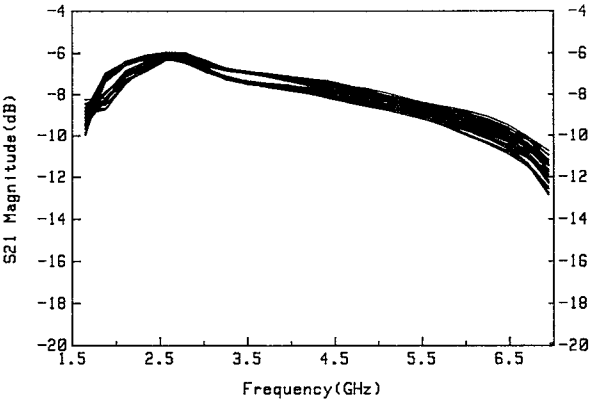

Figure 9. Measured Insertion Gain of Lowband Phase Shifter Chip in All 32 States.

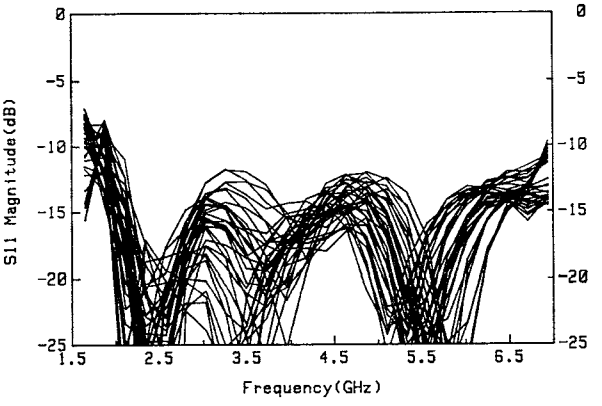

Figure 10. Measured S11 Magnitude of Lowband Phase Shifter Chip in All 32 States.

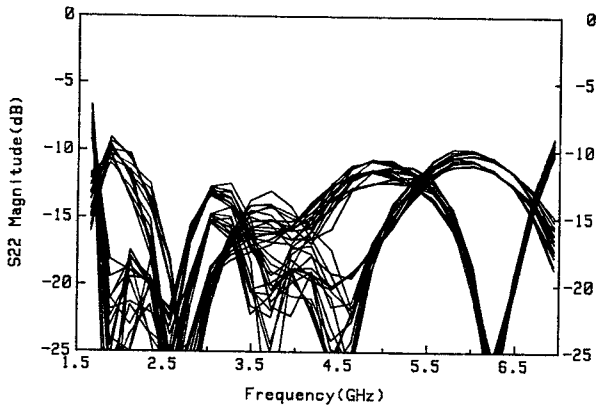

Figure 11. Measured S22 Magnitude of Lowband Phase Shifter Chip in All 32 States.

CONCLUSION

Five bit digitally controlled MMIC phase shifters that cover two octaves of bandwidth have been successfully demonstrated. The phase shifters maintain excellent performance over their entire operational bandwidths.

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